# PROGRAMMABLE SIGNAL TERMINATION FOR FPGAs AND THE LIKE


## ABSTRACT

A termination scheme for the I/O circuitry of a programmable device, such as a field-programmable gate array (FPGA), has programmable resistors switchably connected between reference voltages and two of the device's I/O pads and additional programmable resistors switchably connected between the two I/O pads. By appropriately controlling the reference voltages and the resistance levels, a single implementation of the termination scheme can be used to conform to a relatively wide variety of symmetric and non-symmetric complementary and differential signaling applications.